

#24/E(WG)

PATENT
RECEIVED
OCT - 2 2002
TECHNOLOGY CENTER 2890
10/2/02
John H

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:
HIDAKA, Itsuo

Appl. No.: 09/525,802

Filed: March 15, 2000

For: SEMICONDUCTOR DEVICE

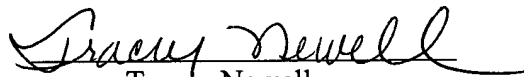
Art Unit: 2827

Examiner: CRUZ, Lourdes

Atty Docket: AKM-00301

CERTIFICATE OF MAILING

I hereby certify that the foregoing document is being deposited with the United States Postal Service as first class mail, postage prepaid, "Post Office to Addressee", in an envelope addressed to: Commissioner of Patents, Washington, DC 20231 on September 24, 2002.


Tracey Newell

AMENDMENT UNDER 37 CFR 1.116

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is being provided in response to the Final Office Action dated July 2, 2002, for the above-captioned U.S. patent application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required for consideration of this paper (including fees for net addition of claims) are authorized to be charged in two originally-executed copies of an Amendment Transmittal Letter filed herewith. Attached herewith is a set of "clean" rewritten claims as required by 37 C.F.R. § 1.121.

Kindly enter the following amendments:

IN THE CLAIMS:

Please amend Claims 1, 2, 5-9, and 13-15 as follows:

1. (Five Times Amended) A semiconductor device having multiple wiring layers,
comprising:

a signal line which is formed in a wiring layer[, and to which a signal voltage is applied];

two adjacent lines which are [so adjacent] oblique to said signal line [as] and not [to be]
connected thereto, and which are formed in the same wiring layer where said signal line is formed;

two intersection lines which are respectively formed in wiring layers, each being present
via an insulating layer above or under the wiring layer where said signal line and said adjacent
lines are formed, and which are formed along a surface area corresponding to an area which is
enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the
insulating layers formed between said adjacent lines and said two intersection lines, along entire
areas of said two adjacent lines, and which respectively and electrically connect said two
adjacent lines and said two intersection lines,

wherein said signal line is completely enclosed by said two adjacent lines, said two
intersection lines, and said entire-line-area through-holes, which are one of conductors and
semiconductors[; and

the electric potentials of said two adjacent lines, said two intersection lines, and said
entire-line-area through holes have at least one of a plurality of electric potential sources having
a selected potential value and a plurality of resistive connections at selected locations to the
signal line such that the electric potential has a same phase as a phase of an electric potential of
said signal line].

2. (Four Times Amended) The semiconductor device according to claim 1, wherein when a signal voltage is applied to the signal line and the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line, said semiconductor device prevents interference from electronic noise [said two adjacent lines are disposed substantially in parallel to said signal line] .

5. (Five Times Amended) A semiconductor device having multiple wiring layers, comprising:

[a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;]

a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers[, and to which signal voltages having a same phase are applied];

two adjacent lines which are disposed adjacent to both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines,

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors, and

[the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the

signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line]

wherein at least one of said plurality of signal lines intersects another signal line in another layer.

6. (Four Times Amended) The semiconductor device according to claim 5, wherein said lines and through-holes are arranged so that when said signal lines have signal voltages having a same phase and when electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said [signal line] plurality of signal lines, said semiconductor device prevents interference from electronic noise.

7. (Twice Amended) The semiconductor device according to claim 5, wherein said lines and through-holes are arranged so that when said signal lines have signal voltages having a same phase and when electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes have a same phase as a phase of an electric potential of said plurality of signal lines, said semiconductor device prevents interference from electronic noise.

8. (Five Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

[a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;]

a plurality of signal lines which are formed not to intersect each other in a same wiring layer[, and to which signal voltage having different phases are applied];

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto and [to be disposed beyond the edge] are formed respectively outside of said selected outer two of the plurality of signal lines, and which are formed in the same wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the same wiring layer where said plurality of signal lines are formed, the second adjacent lines being disposed between each individual one of said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent lines, said at least one second adjacent

line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors; and

wherein at least one of said plurality of signal lines intersects another signal line in a different wiring layer.

9. (Four Times Amended) The semiconductor device according to claim 8, wherein when signal voltages having different phases are applied to said plurality of signal lines and when electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line, said semiconductor device prevents interference from electronic noise.

13. (Five Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

[a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate having at least five wiring layers;]

a first plurality of signal lines which are formed in [the] a second of the wiring layers[, and to which signal voltages are respectively applied];

a second plurality of signal lines which are formed in [the] a fourth of the wiring layers[, and to which signal voltages are respectively applied];

a plurality of adjacent lines, each pair of which are formed either in the second or fourth wiring layer of the wiring layers where said signal lines are formed, respectively adjacent onto both sides of a selected one of said signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a first wiring layer under the second wiring layer of said first plurality of signal lines, or in a fifth wiring layer above the fourth wiring layer of said second plurality of signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said signal lines formed either in the second or fourth wiring layer of said signal lines;

a second intersection line which is formed in a third wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire

areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein each said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein the direction of the first plurality of signal lines [may be] is different from the direction of the second plurality of signal lines in [any] a selected area; and

wherein at least one of: said first plurality of signal lines and said second plurality of signal lines intersects another signal line in a different wiring layer.

14. (Twice Amended) The semiconductor device according to claim 13, wherein when signal voltages which are out of phase with each other are respectively applied to different ones of said plurality of signal lines, said semiconductor device prevents interference from electronic noise.

15. (Twice Amended) The semiconductor device according to claim 14, wherein when electric potentials of said first and second adjacent lines, said first and second intersection lines and said first and second entire-line-area through-holes have a same phase as an electric potential of said signal lines, said semiconductor device prevents interference from electronic noise.

REMARKS

This paper is being provided in response to the July 2, 2002 Final Office Action for the above-referenced application. In this response, Applicant has amended Claims 1, 2, 5-9 and 13-15 to clarify Applicant's invention. Applicant respectfully submits that the modifications to the Claims are supported by the originally-filed application.

Applicant thanks the Examiner for indicating that Claim 16 is allowed.

In response to the objection to the drawings, Applicant has amended the claims in accordance with remarks set forth in the Office Action. In view of the foregoing, Applicant respectfully requests that the objection be reconsidered and withdrawn.

In response to the rejection of Claims 5-15 under 35 U.S.C., first paragraph, Applicant has amended the claims in accordance with remarks set forth in the Office Action. In view of the foregoing, Applicant respectfully requests that the objection be reconsidered and withdrawn.

In response to the rejection of Claims 8 and 9 under 35 U.S.C. 112, second paragraph, Applicant has amended Claim 8 in accordance with remarks set forth in the Office Action. Applicant notes that the Office Action also indicates that Claim 13 includes terms that lack antecedent basis. Accordingly, Applicant has also amended Claim 13 in accordance with remarks set forth in the Office Action. Applicant also notes that the Office Action indicates that some existing claims depend from cancelled claims. Applicant has carefully reviewed the application and finds no existing claim depending from a cancelled claim. In view of the

foregoing, Applicant respectfully request that the Examiner reconsider and withdraw this rejection.

The rejection of Claims 1 and 2 under 35 U.S.C. 102(b) as being anticipated by Cronin et al. (U.S. Patent No. 4,776,087, hereinafter referred to as "Cronin") is traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1 and 2, as amended herein, are patentable over Cronin.

Applicant's Claim 1, as amended herein, recites a semiconductor device having multiple wiring layers. A signal line is formed in a wiring layer. Two adjacent lines are oblique to the signal line and not connected thereto, and which are formed in the same wiring layer where the signal line is formed. Two intersection lines are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where the signal line and the adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by the two adjacent lines. A plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and which respectively and electrically connect the two adjacent lines and the two intersection lines. The signal line is completely enclosed by the two adjacent lines, the two intersection lines, and the entire-line-area through-holes, which are one of conductors and semiconductors. Claim 2 depends from Claim 1.

Cronin relates to a shielded transmission line structure fabricated in VLSI dimensions as well as to a manufacturing method for making such a structure. (Col. 1, Lines 5-7). Cronin discloses a cross-sectional view of a totally shielded transmission line structure compatible with

current integrated circuit metallization techniques. Upper and lower plate structures defined by conductor layers 52 and 60, respectively, are coupled together by peripheral conductor structures defined by layer 56. The peripheral conductor structures are disposed about and spaced from a central conductor structure 56A and the outer conductors are coupled to ground potential. Central conductor 56A is separated from the conductors disposed about its periphery by insulator layers 54 and 58. (Col. 1, Lines 53-66; Figure 6). In combination, the upper plate structure, the peripheral conductor structures and the lower plate structure surround the central conductor and are insulated therefrom by the respective insulator layers. The surrounding conductors are coupled to ground potential, and high frequency transmission signals are propagated along the central conductor. (See Abstract). Conductor 52 can be formed from aluminum, aluminum alloys, refractory metals, refractory metal alloys, doped polysilicon, or various combinations thereof. (Col. 4, Lines 10-13). Conductor layer 56 can be composed of the same materials as layer 52. It is preferred in Cronin's teachings to form layer 56 from a material that can be chemically vapor deposited (CVD) so as to fill the troughs formed in the insulator 54 without creating voids. Refractory metal layers such as tungsten provide good trough filling properties. (Col. 4, Lines 53-64). Cronin's Figure 10 discloses an embodiment wherein separate metal layers are used to fill the troughs defined in the layers 54 and 58. Instead of using a single metal deposition to fill both the trough holes defined in the insulator layer and define a metal line on the upper surface of the insulator layer, separate metal layers are provided. The troughs formed in layers 54 and 58 are filled with metal layers 53 and 57, respectively. Thus, the peripheral conductors are defined by conductor layers 53 and 56, and the upper plate structure is defined by conductor layers 57 and 60. (Col. 5, Lines 20-31).

Applicant's amended Claim 1 is neither disclosed nor suggested by Cronin in that Cronin neither discloses nor suggests *a semiconductor device having multiple wiring layers, comprising: a signal line which is formed in a wiring layer and two adjacent lines which are oblique to said signal line and not connected thereto, and which are formed in the same wiring layer where said signal line is formed*, as set forth in Applicant's amended Claim 1. Cronin's Figure 6 illustrates two conductors 56 which appear to be parallel to central conductor 56A. Cronin neither discloses nor suggests *two adjacent lines which are oblique to said signal line and not connected thereto*, as set forth in Applicant's amended Claim 1.

Applicant's amended Claim 2, which depends from claim 1, recites the additional features of *when a signal voltage is applied to the signal line and the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line, said semiconductor device prevents interference from electronic noise*, which Applicant respectfully submits is also not found in Cronin.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 5-9 and 13-15 under 35 U.S.C. 103(a) as being unpatentable over Cronin in view of Ma (U.S. Patent No. 5,729,047, hereinafter referred to as "Ma") is hereby

traversed and reconsideration thereof is respectfully requested. Applicant's Claims 5-9 and 13-15, as amended herein, are patentable over the references, taken separately or in combination.

Applicant's Claim 5, as amended herein, recites a semiconductor device having multiple wiring layers. A plurality of signal lines are disposed to not intersect each other in a same one wiring layer of the multiple wiring layers. Two adjacent lines are disposed adjacent to both sides of the plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where the plurality of signal lines are formed. Two intersection lines are formed in a wiring layer each being present via insulating layers above or under the wiring layer where the plurality of signal lines and the two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by the two adjacent lines. A plurality of entire-line-area through-holes respectively penetrate through insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and which respectively and electrically connect the two adjacent lines with the two intersection lines. The plurality of signal lines are completely enclosed by the two adjacent lines, the two intersection lines, and the plurality of entire-line-area through-holes, which are one of conductors and semiconductors. At least one of said plurality of signal lines intersects another signal line in another layer. Claims 6 and 7 depend from Claim 5.

Applicant's Claim 8, as amended herein, recites a semiconductor device having multiple wiring layers. A plurality of signal lines which are formed not to intersect each other in a same wiring layer. Two first adjacent lines are so formed adjacent respectively onto a selected outer two of the plurality of signal lines as not to be connected thereto and are formed respectively outside of the selected outer two of the plurality of signal lines, and which are formed in the

same wiring layer where the plurality of signal lines are formed. At least one second adjacent line is formed in the same wiring layer where the plurality of signal lines are formed. The second adjacent lines are disposed between each individual one of the plurality of signal lines so as not to be connected to the plurality of signal lines. The semiconductor device includes two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where the signal lines and the first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by the two first adjacent lines. Entire-line-area through-holes respectively penetrate through insulating layers formed between the first and second adjacent lines and the two intersection lines along entire areas of the first and second adjacent lines, and which respectively and electrically connect the first and second adjacent lines with the two intersection lines. The plurality of signal lines are completely enclosed by the two first adjacent lines. The at least one second adjacent line, the two intersection lines, and the entire-line-area through-holes are one of semiconductors and conductors. At least one of the plurality of signal lines intersects another signal line in a different wiring layer. Claim 9 depends from Claim 8.

Applicant's Claim 13, as amended herein, recites a semiconductor device having multiple wiring layers. A first plurality of signal lines are formed in a second of the wiring layers. A second plurality of signal lines which are formed in a fourth of the wiring layers. The semiconductor device includes a plurality of adjacent lines, each pair of which are formed either in the second or fourth wiring layer of the wiring layers where the signal lines are formed, respectively adjacent onto both sides of a selected one of the signal lines which is formed in an identical layer, thereby not to be connected to the selected one of the plurality of signal lines. Two first intersection lines are each formed either in a first wiring layer under the second wiring

layer of the first plurality of signal lines, or in a fifth wiring layer above the fourth wiring layer of the second plurality of signal lines, and each of which is formed along a surface area corresponding to an area enclosed by the pair of adjacent lines formed on the both sides of a corresponding one of the signal lines formed either in the second or fourth wiring layer of the signal lines. A second intersection line is formed in a third wiring layer formed between the wiring layers of the signal lines, and which is formed along a surface area corresponding to at least one area enclosed by the pair of adjacent lines. A plurality of first entire-line-area through-holes penetrate through insulating layers respectively formed between the adjacent lines and the first intersection lines, along entire areas of the adjacent lines, thereby electrically connecting the adjacent lines with the two first intersection lines. A plurality of second entire-line-area through-holes penetrate through insulating layers respectively formed between the adjacent lines and the second intersection line, along entire areas of the adjacent lines, thereby electrically connecting the adjacent lines with the second intersection line. Each of the plurality of signal lines are completely enclosed by the plurality of adjacent lines, the two first intersection lines, the second intersection line, the plurality of first entire-line-area through-holes, and the plurality of second entire-line-area through-holes, which are one of conductors and semiconductors. The direction of the first plurality of signal lines is different from the direction of the second plurality of signal lines in a selected area. At least one of: the first plurality of signal lines and the second plurality of signal lines intersects another signal line in a different wiring layer. Claims 14 and 15 depend from Claim 13.

Cronin is summarized above.

Ma relates generally to integrated circuit devices, and in particular relates to a method and structure for providing signal isolation and decoupling in an integrated circuit device, such as random access memory devices. (Col. 1, Lines 8-12). Ma discloses a signal isolation and decoupling structure fabricated in an integrated circuit device for providing signal isolation and decoupling for signal carrying conductors of the device. One of the conductors is embedded in a dielectric material and enclosed within an isolation structure of an electrically conductive material which is formed in the integrated circuit device and extends substantially the length of the conductor. The isolation structure includes top and bottom walls of electrically conductive material and first and second side walls also of an electrically conductive material which electrically interconnect the top and bottom walls forming a closure around the conductor. (See Abstract).

Figures 2-4 of Ma disclose a conductor 90 surrounded by an enclosure 100 that extends over a portion of the integrated circuit device, along at least a portion of, and preferably along substantially the entire length or extent of the conductor 90. The isolation structure has a top wall 102, a bottom wall 104, and side walls 106 and 108. (Col. 4, Lines 62- Col. 5, Line 6). The interior of the enclosure 100 is filled with a dielectric material. (Col. 5, Lines 41-42). Walls 102 and 104 are made of a metal, preferably aluminum. (Col. 5, Lines 56-57). The side walls are made of a metal, preferably tungsten or other highly conductive materials. (Col. 5, Lines 60-61). The conductive layer that forms the top wall 102 is connected to the ground or Vss for the device 90 or any reference voltage that is stable. Alternatively, the bottom wall 104 and/or both of the side walls 106 and 108 can be connected to ground or a source of reference potential. (Col. 6, Lines 59-65). Ma's Figure 16 discloses an enclosure 160 having four cells 161-164 which are arranged in a two-by-two matrix for isolating four signal carrying conductors 171-174 from one

another and from other conductors (not shown) located external to the isolation structure. (Col. 9, Lines 30-36).

Applicant's Claim 5, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a semiconductor device having multiple wiring layers, comprising: a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers, wherein at least one of said plurality of signal lines intersects another signal line in another layer,*** as set forth in Applicant's amended Claim 5. Cronin discloses a shielded transmission line. Ma discloses a signal isolation and decoupling structure arranging four conductors in a two-by-two matrix isolating each of the conductors from one another (Ma's Figure 16), and for enclosing a plurality of conductors within isolation (Ma's Figure 17). However, neither of the references, taken separately or in combination, disclose or suggest ***a semiconductor device having multiple wiring layers, comprising: a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers, wherein at least one of said plurality of signal lines intersects another signal line in another layer,*** as set forth in Applicant's amended Claim 5.

Applicant's amended Claims 6 and 7 that depend from Claim 5 are patentable for at least the same reasons as Claim 5 and each of Claims 6 and 7 recite additional structural features. In particular, Claim 6 recites the additional structural feature of ***said lines and through-holes are arranged so that when said signal lines have signal voltages having a same phase and when electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value***

independent of an electric potential applied to said plurality of signal lines, said semiconductor device prevents interference from electronic noise.

For reasons similar to those set forth regarding Claim 5, Applicant's amended Claim 8 is neither disclosed nor suggested by the references, taken separately or in combination.

In particular, Applicant's Claim 8, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that neither of the references, alone or in combination, disclose or suggest *a semiconductor device having multiple wiring layers, said device comprising: a plurality of signal lines which are formed not to intersect each other in a same wiring layer, wherein at least one of said plurality of signal lines intersects another signal line in a different wiring layer*, as set forth in Applicant's amended Claim 8.

Applicant's amended Claim 9 which depends from Claim 8 is patentable for at least the same reasons as Claim 8. Claim 9 recites the additional feature *when signal voltages having different phases are applied to said plurality of signal lines and when electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line, said semiconductor device prevents interference from electronic noise*, as set forth in Applicant's amended Claim 9.

For reasons similar to those set forth regarding Claim 5, Applicant's amended Claim 13 is neither disclosed nor suggested by the references, taken separately or in combination.

Applicant's Claim 13, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest *a semiconductor device having multiple wiring layers, said device comprising: a first plurality of signal lines which are formed in a second of the wiring layers, a second plurality of signal lines which are formed in a fourth of the wiring layers, wherein the direction of the first plurality of signal lines is different from the direction of the second plurality of signal lines in a selected area; and wherein at least one of: said first plurality of signal lines and said second plurality of signal lines intersects another signal line in a different wiring layer*, as set forth in Applicant's amended Claim 13.

Applicant's Claims 14 and 15, which depend from Claim 13, are patentable for at least the same reasons as Claim 13 and recite additional features. In particular, Claim 14 recites the additional feature of *when signal voltages which are out of phase with each other are respectively applied to different ones of said plurality of signal lines, said semiconductor device prevents interference from electronic noise*, as set forth in amended Claim 14.

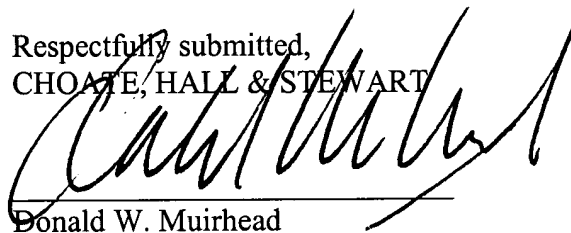
In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

September 24, 2002
Date

Patent Group
Choate, Hall & Stewart
Exchange Place
53 State Street
Boston, MA 02109

Respectfully submitted,
CHOATE, HALL & STEWART



Donald W. Muirhead
Reg. No. 33,978

CLAIMS

Following are a set of clean, rewritten Claims in accordance with amendments made herein.

1. (Five Times Amended) A semiconductor device having multiple wiring layers, comprising:
 - a signal line which is formed in a wiring layer;
 - two adjacent lines which are oblique to said signal line and not connected thereto, and which are formed in the same wiring layer where said signal line is formed;
 - two intersection lines which are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and
 - a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines,wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines, and said entire-line-area through-holes, which are one of conductors and semiconductors.

2. (Four Times Amended) The semiconductor device according to claim 1, wherein when a signal voltage is applied to the signal line and the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have at least one of a plurality of electric potential sources having a selected potential value and a plurality of resistive connections at selected locations to the signal line such that the electric potential has a same phase as a phase of an electric potential of said signal line, said semiconductor device prevents interference from electronic noise.

5. (Five Times Amended) A semiconductor device having multiple wiring layers, comprising:

a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers;

two adjacent lines which are disposed adjacent to both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines,

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein at least one of said plurality of signal lines intersects another signal line in another layer.

6. (Four Times Amended) The semiconductor device according to claim 5, wherein said lines and through-holes are arranged so that when said signal lines have signal voltages having a same phase and when electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said plurality of signal lines, said semiconductor device prevents interference from electronic noise.

7. (Twice Amended) The semiconductor device according to claim 5, wherein said lines and through-holes are arranged so that when said signal lines have signal voltages having a same phase and when electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes have a same phase as a phase of an electric potential of said plurality of signal lines, said semiconductor device prevents interference from electronic noise.

8. (Five Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of signal lines which are formed not to intersect each other in a same wiring layer;

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto and are formed respectively outside of said selected outer two of the plurality of signal lines, and which are formed in the same wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the same wiring layer where said plurality of signal lines are formed, the second adjacent lines being disposed between each individual one of said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent lines, said at least one second adjacent line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors; and

wherein at least one of said plurality of signal lines intersects another signal line in a different wiring layer.

9. (Four Times Amended) The semiconductor device according to claim 8, wherein when signal voltages having different phases are applied to said plurality of signal lines and when electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line, said semiconductor device prevents interference from electronic noise.

13. (Five Times Amended) A semiconductor device having multiple wiring layers, said device comprising:

a first plurality of signal lines which are formed in a second of the wiring layers;

a second plurality of signal lines which are formed in a fourth of the wiring layers;

a plurality of adjacent lines, each pair of which are formed either in the second or fourth wiring layer of the wiring layers where said signal lines are formed, respectively adjacent onto both sides of a selected one of said signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a first wiring layer under the second wiring layer of said first plurality of signal lines, or in a fifth wiring layer above the fourth wiring layer of said second plurality of signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said signal lines formed either in the second or fourth wiring layer of said signal lines;

a second intersection line which is formed in a third wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along

entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein each said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors, and

wherein the direction of the first plurality of signal lines is different from the direction of the second plurality of signal lines in a selected area; and

wherein at least one of: said first plurality of signal lines and said second plurality of signal lines intersects another signal line in a different wiring layer.

14. (Twice Amended) The semiconductor device according to claim 13, wherein when signal voltages which are out of phase with each other are respectively applied to different ones of said plurality of signal lines, said semiconductor device prevents interference from electronic noise.

15. (Twice Amended) The semiconductor device according to claim 14, wherein when electric potentials of said first and second adjacent lines, said first and second intersection lines and said first and second entire-line-area through-holes have a same phase as an electric potential of said signal lines, said semiconductor device prevents interference from electronic noise.